**ECE -1 Lab **

**Experiment - 3**

**Aim:** Implementation of 2x1, 4x1 and 8x1 multiplexers using dataflow, behavioral and structural modeling in VHDL.

Description:

Part1:

1. Implement a 2x1 multiplexer using dataflow modeling.
2. Implement a 2x1 multiplexer using behavioral modeling using case statement.
3. Implement a 4x1 multiplexer using dataflow modeling.
4. Implement a 4x1 multiplexer using structural modeling and using only 2x1 MUX.
5. Implement an 8x1 MUX using structural modeling and using 4x1 and 2x1 MUX.

Part2:

1. For each type of the above implementations generate the synthesis report.
2. Make one appropriate testbench waveform file for each experiment and verify the testbench.
3. Compare delay, power and cell usage for each type of multiplexers.